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REMARKS

Claims 1-20 are currently pending. In the Office Action, claims 1-2, 7-8, 14-15 and 18-20 were rejected under 35 U.S.C. §102(b) as being anticipated by US Pat. No. 6,184,660 to Hatular (hereinafter "Hatular"), and claims 5-6 and 12-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hatular in view of US Pat. No. 6,894,461 to Hack et al. (hereinafter "Hack").

Claims 3-4, 9-11 and 16-17 were objected to as being dependent upon a rejected base claim but were otherwise considered allowable.

Applicant respectfully traverses the §102(b) rejection of claims 1-2, 7-8, 14-15 and 18-20 as being anticipated by Hatular.

The reliance on Hatular to sustain an anticipatory rejection of claims 1, 7 and 14 is misplaced. As described in his Abstract, Hatular discloses a "battery charger IC for controlling operation of a buck converter circuit that includes a series switch and a resistor for sensing battery charging current." FIGs 1A and 1B of Hatular both depict a PWM buck converter circuit 60 (col. 6, lines 10-15, and see col. 4, lines 57-62). The battery charger IC 50 includes a switch drive 162 that supplies signals for controlling the operation of the PWM buck converter circuit 60; the switch drive 162 supplies, via a HDR signal line 164 to an input of an inverting amplifier 66, a signal for turning the series switch 62 on and then off; and the switch drive 162 supplies a signal for turning the synchronous-rectifier switch 76 first off and then on via a LDR signal line 166. (Hatular col. 12, lines 8-15). The series switch 62 is described as a P-type MOSFET (col. 6, line 17) and the synchronous-rectifier switch 76 is described as an N-type MOSFET (col. 6,

line 57), so both are switching FETs. The drain terminals 62d and 76d of the switches 62 and 76, respectively, are shown in FIGS. 1A and 1B coupled together and to one end of an inductor 68. As described in Hatular (col. 7, lines 11-20), a current-sensing resistor 82 connects in series with the inductor 68 at the junction between the inductor 68 and a filter capacitor 72. And also the voltages present respectively at opposite terminals of the current-sensing resistor 82 during charging of a smart battery 22 are supplied through isolation resistors 84p and 84m to the battery charger IC 50, shown as inputs ICHP and ICHM. The IC 50 includes a charging-current sense amplifier 218 having positive and negative inputs receiving the ICHP and ICHM inputs, respectively, and having an output coupled to the sample-and-hold circuit 214 (Hatular, FIG. 2 and col. 14, lines 47-50)

As understood by those skilled in the art, the node coupling the drain terminals 62d and 76d of the switching devices 62 and 76, respectively, is the phase node for a buck type converter. This phase node effectively switches between ground (or thereabouts) and the input voltage provided at the source 62s of the switch 62, where the switched voltage is applied to the inductor 68. The other side of the inductor 68 is coupled to the filter capacitor 72, which generally develops a fixed output voltage level. Thus, the nodes on either side of the sense resistor 82 are not phase nodes. When the smart battery 22 is being charged, current flows through the sense resistor 82 and the charging-current sense amplifier 218 senses the voltage *across* the sense resistor 82 (and thus current through the sense resistor 82), rather than sensing voltage of a phase node.

Contrary to that stated in the Office Action, the sample circuit of claim 1 does not read on Hatular including Hatular's sample-and-hold circuit 214. First, the sample-and-hold circuit 214 does not sample voltage of a phase node at any time, including the first

phase of the PWM signal. Instead, it senses a voltage across the sense resistor 82 for sampling charging current of the smart battery 22. Second, Hatular's sample-and-hold circuit 214 does not provide a sum voltage indicative of the initial phase voltage added to the voltage level of the phase node during the second phase of the PWM signal.

Furthermore, Hatular's comparators 192 and 196 are not coupled to the sample-and-hold circuit 214 and do not compare the sum voltage of the sample circuit with a predetermined reference voltage. And the output of the comparators 192 and 196 do not provide an output indicative of an activation state of the lower switch 76 during the second phase of the PWM signal. Instead, the comparators 192 and 196 sense the VIN signal (from voltage divider 64 sensing voltage of source terminal 62s of the switch 62) and the VFB signal (from voltage divider 92 sensing voltage of battery-charging-current line 88) for providing signals to an under-and-over voltage-protection circuit 188 within the IC 50 for purposes of determining the appropriate conditions for charging the smart battery 22. The comparators 192 and 196 and associated circuitry in Hatular have nothing whatsoever to do with determining the activation state of the FET switch 76.

Applicant respectfully submits, therefore, that claim 1 is allowable over Hatular. Claim 2 is allowable as depending upon allowable claim 1. Applicant requests withdrawal of this rejection.

And further with respect to claim 2, Hatular does not show a switch circuit that samples a predetermined reference voltage during the first phase of the PWM signal and that applies a first voltage indicative of the predetermined reference voltage to the first input of the comparator during the second phase of the PWM signal. And Hatular does

not show the sample circuit being operative to sample a second voltage indicative of the initial voltage of the phase node during the first phase of the PWM signal, that determines the sum voltage by adding the second voltage to the voltage level of the phase node during the second phase of the PWM signal, and that applies the sum voltage to the second input of the comparator as recited in claim 2.

Claim 7 is allowable over Hatular for similar reasons recited above for claim 1. Hatular does not show or describe a rectified synchronous FET power regulator including a comparator circuit coupled to the phase node for detecting the activation state of the lower FET as described in claim 7. In particular, Hatular does not show or describe the comparator circuit including a sample circuit which samples an initial voltage of the phase node during a first state of the PWM signal and that provides a sum voltage indicative of the sum of the initial voltage and the voltage level of the of the phase node during a second state of the PWM signal as recited in claim 7. And Hatular does not show or describe the comparator circuit including a comparator that compares the sum voltage with a predetermined reference voltage and that provides an output indicative of the activation state of the lower FET as recited in claim 7.

Applicant respectfully submits, therefore, that claim 7 is allowable over Hatular. Claim 8 is allowable as depending upon allowable claim 7. Applicant requests withdrawal of this rejection.

Claim 14 is allowable over Hatular for similar reasons recited above for claims 1 and 7. Hatular does not show storing a voltage level indicative of the initial voltage level of a phase node while the lower FET is turned on. Hatular does not detect the phase node

voltage and the only storage noted in the Office Action in regard to Hatular relates to sampling a voltage indicative of charging current as sensed by the resistor 82 on the other side of the inductor 68. And Hatular does not show determining when the voltage level of the phase node falls below the initial voltage level by a predetermined amount after a FET driver initiates turning off the lower FET as recited in claim 14. Hatular, therefore, has nothing whatsoever to do with detecting the activation state of a switching FET as recited in claim 14.

Applicant respectfully submits, therefore, that claim 14 is allowable over Hatular. Claims 15 and 18-20 are allowable over Hatular as depending upon an allowable base claim. Applicant requests withdrawal of this rejection.

And further with respect to claim 18, Hatular does not show switching a second end of a first capacitor to a first input of a comparator, switching a first end of a second capacitor to ground, and switching a second end of the second capacitor to a second input of the comparator.

And further with respect to claim 19, Hatular does not appear to address initial ringing at all, much less ignoring such ringing.

And further with respect to claim 20, although Hatular's switches 62 and 76 alternatively switch according to PWM operation, Hatular does not address turning off the lower FET when the voltage of the phase node falls below the initial voltage level by the predetermined amount. In fact, the freewheeling zener diode 74 might prevent such voltage level change and detection thereof in the first place.

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Applicant respectfully traverses the §103(a) rejection of claims 5-6 and 12-13 as being unpatentable over Hatular in view of Hack.

Concerning claim 5, it was stated in the Office Action that claim 4 was only objected to as depending on a rejected claim but was otherwise allowable. And since claim 5 depends on claim 4, claim 5 should also have been objected to rather than being rejected. Applicant requests withdrawal of this rejection as improper.

The rejection of claim 12 is improper for the same reason cited above for claim 5. It was stated in the Office Action that claim 11 was only objected to as depending on a rejected claim but was otherwise allowable. And since claim 12 depends on claim 11, claim 12 should also have been objected to rather than being rejected. Applicant requests withdrawal of this rejection as improper.

The §103(a) rejection of claims 5-6 and 12-13 is premised on Hatular disclosing the inventions of claims 1 and 7, so that this rejection has already been overcome since Hatular does not show or describe the inventions of claims 1 or 7 as described above. And Hack does not overcome the noted limitations of Hatular with respect to claims 1 or 7. In this manner, claims 5 and 6 are allowable over Hatular in view of Hack as depending upon allowable claim 1, and claims 12 and 13 are allowable over Hatular in view of Hack as depending upon claim 7. Applicant requests withdrawal of this rejection.

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CONCLUSION

Applicant respectfully submits that for the reasons recited above and for various other reasons, the claims are allowable and the objections and rejections should be withdrawn. Reconsideration of the rejections and objections are respectfully requested. Should this response be considered inadequate or non-responsive for any reason, or should the Examiner have any questions, comments or suggestions that would expedite the prosecution of the present case to allowance, Applicants' undersigned representative earnestly requests a telephone conference.

Respectfully submitted,

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